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Enhance FPGA-based Systems with Programmable Oscillators

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ESC-3027

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Outline

- FPGA clocking
- Programmable clocks
- Dynamic programmable oscillators
- EMI reduction
- Conclusions

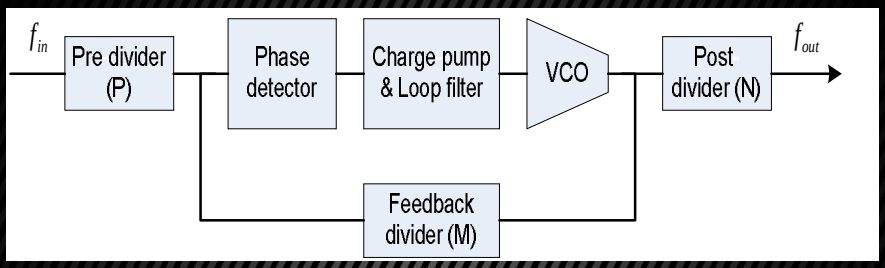
FPGA Clocking

- FPGA designs use multiple clocks to drive different blocks
  - Each may require a different frequency
- External and internal clocks
  - Dependent on clock speed and jitter requirements

Clocking Speed

- Multiple standard frequencies for different applications
  - 100 MHz for PCI Express
  - 75 MHz for SATA
  - 33.333 MHz for PCI
- Clock speeds for processors or state-machine engines can usually be selected
  - Optimize speed, power or resource usage
- Combination of external oscillators and internal PLLs

Typical Integer PLL



Output frequency is defined by Equation 1:

$$f_{out} = \left(\frac{f_{in}}{P}\right)\left(\frac{M}{N}\right)$$

PLL Bandwidth

- Maximum PLL bandwidth is a function of phase detector update rate

$$BW_{PLL} < \frac{f_{in}}{10P}$$

- More practical limit:

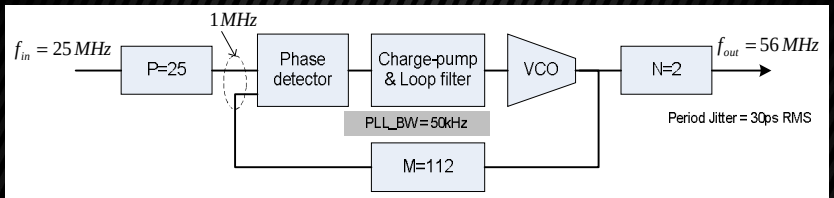
$$BW_{PLL} < \frac{f_{in}}{20P}$$

- Large P à High frequency resolution, Lower PLL bandwidth

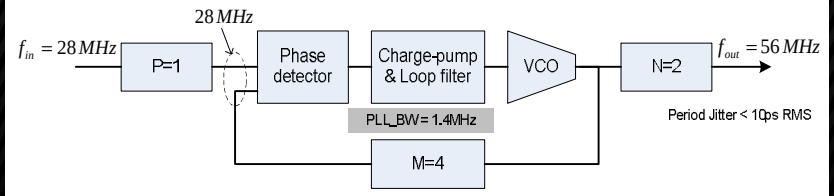
Optimizing PLL Design

- Programmable oscillator as an external reference
  - Lower demand on the internal PLL
  - High frequency resolution
    - Reduce required pre-divide ratios
    - Higher PLL bandwidth
  - Low jitter

Optimizing PLL Design



Standard Frequency Reference Clock



Flexible Frequency Reference Clock

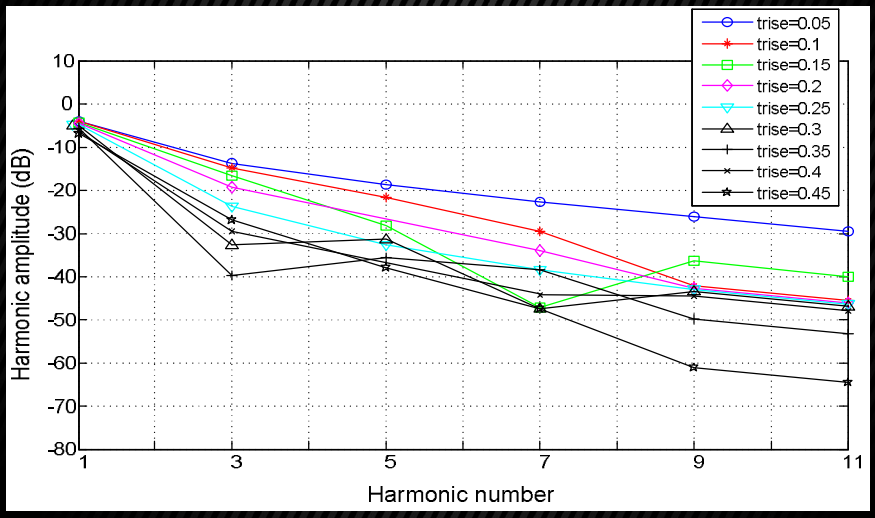
Higher PLL bandwidth and lower jitter

EMI Reduction in FPGA Devices

- Edge rate tuning with programmable oscillators
  - Increase the rise and fall time of the clock signal
  - Reduces EMI generated by higher order clock harmonics radiated from the clock traces in a specific circuit
  - The peak clock signal remains constant, avoiding the voltage swing reduction

Clock Signal Harmonic Amplitude

A function of rise/fall time



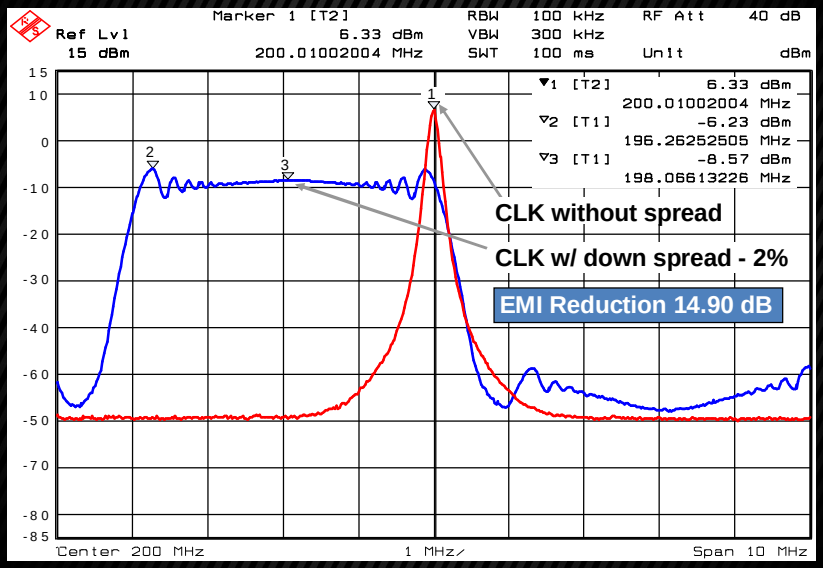
Rise/Fall Time Control for EMI Reduction

- Edge rate adjustment methods
  - Increase load capacitance
    - Increases current consumption
  - Adjusting output current drive with programmable oscillators
    - Does not affect current consumption
- Drive strength tuning for EMI reduction
  - Only works on one circuit at a time
  - Only on clock harmonics radiated from the clock traces
  - May not be possible in high-speed systems

Spread-spectrum Clocking (SSC)

- Reduce peak electromagnetic radiation emitted from the clock tree and data lines clocked with the clock tree
- Spread energy of the clock signal over larger frequency range
  - Reduces peak power at a given frequency
  - Effective for both the primary carrier frequency and higher harmonics
- The higher the clock frequency, the greater the EMI reduction
  - Good solution for high frequency applications
- Frequency spread options
  - Center spread: centered around the carrier frequency
  - Down-spread: modulation is concentrated below the nominal frequency
- Especially good for FPGAs
  - Reduces EMI from all functional blocks with the same clock source
  - Trace filtering and rise/fall time control decrease EMI only in certain sections

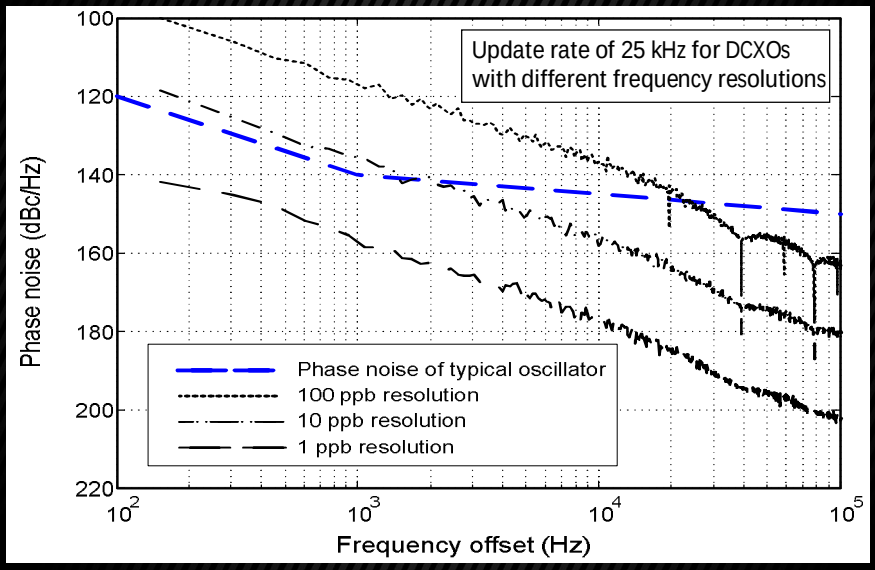
SSC Modulation to Reduce EMI



In-system Frequency Programming

- Digitally controllable oscillators (DCXOs)
  - Superior frequency control
  - Directly driving digital input of the PLL feedback divider or frac-N PLL modulator
  - Jitter clean-up in networking, telecom, video/audio or instrumentation
- DCXOs & FPGAs enable dynamic control of loop bandwidth
  - Bandwidth can be set higher to reduce locking time and improve tracking dynamics
  - Or set lower for better jitter clean-up performance
- Important parameters
  - Frequency resolution
  - Update rate
  - Update delay
- DCXO quantization noise is related to frequency resolution and update rate
  - Should be well below the native phase noise of the oscillator

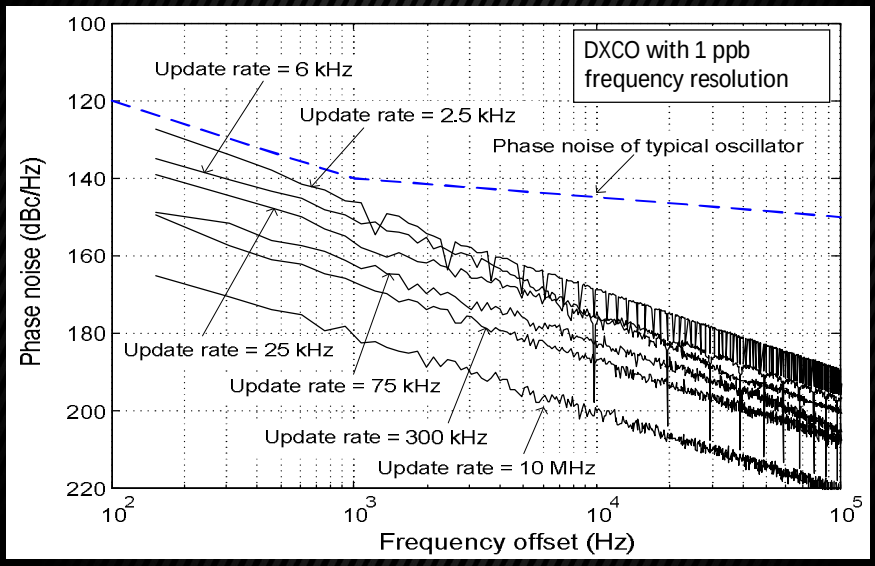
Quantization-induced Phase Noise



Update Rate Effect on Phase Noise

- Typically, low update rates causes error signals from the phase detector and loop filter to be integrated by the DCXO over a longer time, which results in higher phase noise
- DCXO (1 ppb resolution) update rates as low as 2500 updates/s can be tolerated without impact on phase noise
- The update rate and delay of the DCXO contribute to the overall stability of the loop filter
  - When both the update rate and inverse of the update delay are at least 10 times higher that the target loop bandwidth, the loop will be stable
  - This means that for a 1 kHz loop bandwidth, the update rate should be higher than 10 kHz and the update delay shorter than 100 µs

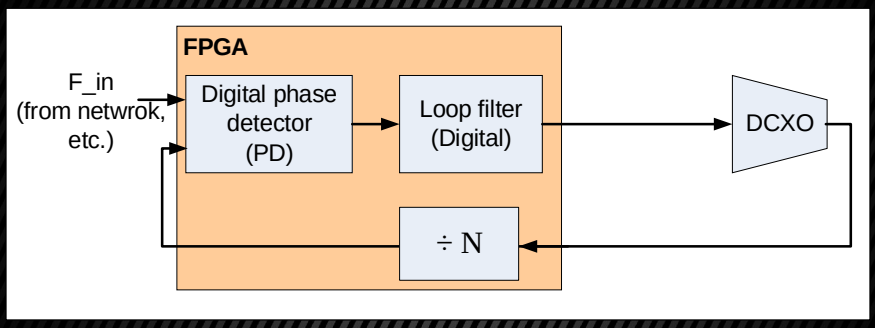
Update Rate Effect on Phase Noise



Jitter Clean-up

- Jitter clean-up techniques needed when locking to a noisy system clock to generate a stable clock signal with low phase noise and low jitter
- High precision oscillators for synchronization or jitter clean-up PLLs
  - Analog (VCXO)
  - Digital (DCXO)
    - Designed to reduce quantization noise
    - Solution for low bandwidth PLLs

FPGA and DCXO Jitter Cleaner



Conclusion

- Programmable oscillators add flexibility and performance to FPGA-based systems
- EMI control with rise/fall adjustment and SSC
- FPGA + dynamically-programmable oscillators
  - Low bandwidth PLLs for jitter cleaning and synchronization
  - Lower cost/size, higher flexibility

Timing Topics at Design East

- Clock Architectures and their Impact on System Performance and Reliability
  - Session Code: ESC-2001
  - Track: Analog & Mixed Signal Design
  - Date/Time: 9/18/2012, 8:00:00 - 9:15:00 AM
  - Location: 202
- How Environmental Forces Impact System Reliability
  - Session Code: ESC-2013
  - Track: Analog & Mixed Signal Design
  - Date/Time: 9/18/2012, 2:00:00 - 3:00:00 PM
  - Location: 202
- Analysis of High-Stability Controlled Oscillators for Low-Bandwidth PLLs
  - Session Code: ESC-2027
  - Track: Analog & Mixed Signal Design
  - Date/Time: 9/18/2012, 4:30:00 - 5:30:00 PM
  - Location: 202
- Enhance FPGA-based Systems with Programmable Oscillators
  - Session Code: ESC-3027
  - Track: Programmable Devices
  - Date/Time: 9/19/2012, 4:30:00 - 5:30:00 PM
  - Location: 202

Contact SiTime

- Thank You!
- Interested? Questions?
- Contact SiTime at sales@sitime.com or Sassan Tabatabaei at stabatabaei@sitime.com